REMARKS

This Amendment responds to the Office Action mailed January 14, 2005 in the above-identified application. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1-56 were previously pending in the application. Claims 18-32, 40-46 and 48-56 have been withdrawn from consideration as directed to a non-elected invention. By this amendment, claims 1, 33-35, 37-39 and 47 have been amended. Claims 11-13 have been canceled without prejudice or disclaimer. Accordingly, claims 1-10, 14-17, 33-39 and 47 are currently under consideration, with claims 1, 33 and 47 being independent claims. No new matter has been added.

The Examiner has rejected claims 1-8, 14, 15, 33-35, 37-39 and 47 under 35 U.S.C. §102(b) as anticipated by Windrem et al. (US 5,574,662). Claims 9-13, 16, 17 and 36 are rejected under 35 U.S.C. §103(a) as unpatentable over Windrem et al. in view of the admitted prior art. The rejections are respectfully traversed.

The Windrem patent discloses a digital video recorder that employs a cache in conjunction with an array of disk drives for recording and playing video signals. Data coming in or going out is buffered in the cache through a cache management algorithm, thereby compensating for periods when the disks may be unable to transfer data (col. 1, lines 43-55). The digital video recorder shown in Fig. 1 of Windrem includes input/output data channels 19, transfer control 18, cache 14, disk array 12, disk controller 13 and control system 16. The cache includes multiple dual-port memories, one memory for each disk drive in the disk array, each memory having a DMA controller. From the point of view of each disk controller, its portion of memory within the cache is independent of the other cache memory portions (col. 2, lines 49-55).

Amended claim 1 is directed to a cache memory system comprising an associative cache including a plurality of memory of locations to store data and addresses associated with the data, a first controller that controls access to the plurality of memory locations by a first device, a second controller that operates independently of the first controller and controls access to the plurality of memory locations by a second device, an address input for selecting memory locations to be accessed, at least one first multiplexer that selects addresses to be provided to the

address input from among addresses provided by the first device and addresses provided by the second controller, an address output for outputting addresses retrieved from memory locations along with data associated therewith, and at least one second multiplexer that selects external address to be provided to the second device from among the addresses provided at the address output and external addresses provided by the second controller.

Initially, it is noted that Windrem discloses a conventional memory that is utilized as a cache buffer for operation with a disk array. The Windrem memory stores only data. By contrast, amended claim 1 is directed to a cache memory system including an associative cache having a plurality of memory locations to store data and addresses associated with the data. Because the associative cache stores both data and addresses associated with the data, it operates in a very different way from a conventional memory as disclosed by Windrem. Windrem does not disclose or suggest an associative cache including a plurality of memory locations to store both data and addresses associated with the data. Accordingly, Windrem describes a very different memory system.

Limitations similar to the limitations of claims 11 and 13 have been incorporated into amended claim 1. It is clear that Windrem does not disclose or suggest a first multiplexer that selects addresses to be provided to the address input as claimed and a second multiplexer that selects external addresses to be provided to the second device as claimed. The Examiner has rejected claims 11 and 13 as unpatentable over Windrem in view of the admitted prior art. Applicants must respectfully disagree.

It is submitted that the combination of Windrem and the admitted prior art is improper. It is well established that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art (MPEP §2143.01). In the present rejection, Windrem relates to a conventional memory used as a cache buffer whereas the admitted prior art relates to an associative cache. In Windrem, each disk controller has a portion of memory within cache 14 that is independent of the other cache memory portions (column 2, lines 52-55). Therefore, one of skill in the art would have no reason to combine the teachings of Windrem and the admitted prior art. The references contain no

teaching or suggestion to make the asserted combination. For this reason the combination of Windrem and the admitted prior art is improper and should be withdrawn.

Assuming, for the sake of argument, that Windrem is properly combinable with the admitted prior art, the references do not teach or suggest all the claim limitations. Amended claim 1 requires at least one first multiplexer that selects addresses to be provided to the address input from among addresses provided by the first device and addresses provided by the second controller. As shown in prior art Fig. 2 of the subject application, multiplexer 218 selects a core read address, a core write address or a memory load address, all of which are provided by the core processor. Thus, the multiplexer 218 shown in prior art Fig. 2 does not select addresses from among addresses provided by the first device and addresses provided by the second controller, as required by amended claim 1.

Furthermore, prior art Fig. 2 of the subject application does not disclose at least one second multiplexer that selects external addresses to be provided to the second device from among addresses provided at the address output and external addresses provided by the second controller. Multiplexer 224 shown in prior art Fig. 2 selects addresses from different ways of the tag array. Multiplexer 230a selects addresses from a copyback buffer 214 and a write buffer 216, both of which are controlled by the cache controller 208. Accordingly, prior art Fig. 2 of the present application does not disclose or suggest a second multiplexer that selects external addresses to be provided to the second device from among the addresses provided at the address output and external addresses provided by the second controller, as required by amended claim 1.

Applicants do not deny that multiplexers are used in virtually every digital design. However, amended claim 1 is directed to a cache memory system wherein multiplexers are utilized to permit a single-port associative cache memory to operate with first and second controllers and to achieve enhanced performance. By contrast, Windrem discloses a dual-port conventional memory rather than an associative cache memory, and the admitted prior art describes a conventional associative cache memory.

For these reasons amended claim 1 is clearly and patentably distinguished over Windrem, taken individually or in combination with the admitted prior art. Claims 2-10 and 14-17 depend from claim 1 and are patentable over the cited prior art for at least the same reasons.

Amended claim 33 is directed to a method comprising selecting addresses to be provided to an address input of an associative cache from among addresses provided by a first device and

addresses provided by a second device, accessing memory locations within the associative cache based upon the selected addresses provided to the address input of the associative cache, outputting addresses retrieved from memory locations of the associative cache along with data associated therewith, and selecting external addresses to be provided to the first device from among addresses output from the associative cache and external addresses provided by the second device.

Amended claim 33 contains method limitations that parallel the apparatus limitations of amended claim 1. Amended claim 33 is clearly patentable over Windrem, taken individually or in combination with the admitted prior art, for the reasons discussed above in connection with claim 1. Further, Applicants respectfully submit that the combination of Windrem and the admitted prior art is improper and should be withdrawn. For these reasons, amended claim 33 is clearly and patentably distinguished over the cited prior art. Claims 34-39 depend from claim 33 and are patentable over the cited prior art for at least the reasons discussed above in connection with claims 1 and 33.

Amended claim 47 is directed to a cache memory system and contains means plus function limitations that parallel the method limitations of claim 33. Amended claim 47 is patentable over Windrem, taken individually or in combination with the admitted prior art, for at least the reasons discussed above in connection with claims 1 and 33.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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